REMARKS

Claims 1, 4-12, and 15-16 are pending in the present application. In the Office Action, claims 1, 4, 11, and 12 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Kodaira, et al (U.S. Patent No. 4,835,734) in view of Bourekas et al (U.S. Patent No. 5,386,579). Claims 5-9 and 15-16 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Kodaira in view of Bourekas and further in view of Christenson, et al (U.S. Patent No. 6,574,721). The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes

that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

With regard to independent claims 1, 11, and 12, Applicants describe and claim receiving a virtual address, comparing at least a portion of the virtual address to a first preselected range, and using a paging mechanism to generate a first physical address from the virtual address in response to the virtual address being outside the first preselected range. Applicants also describe and claim using a hard mapped mechanism to generate a second physical address from the virtual address in response to the virtual address being within the first preselected range. As defined at lines 3-7 on page 9 of the Patent Application, "hard mapping" comprises locating the physical addresses (which are stored in a locked page translation mechanism by a secure kernel) corresponding to the virtual addresses falling within a preselected range at a particular location in physical memory that does not vary during the operation of the data processor (*i.e.*, no swapping occurs).

The aforementioned claimed invention must be considered as a whole for purposes of determining obviousness. A mere selection of various bits and pieces of the claimed invention from various sources of prior art does not render a claimed invention obvious, unless there is a suggestion or motivation in the prior art for the claimed invention, when considered as a whole. In this case, it is respectfully submitted that the obviousness rejection is improper because the Examiner has merely selected bits and pieces from various references and alleged, without record support, that it would have been obvious to combine these pieces to arrive at Applicants'

claimed invention. Applicants respectfully disagree and note that, even considering all the art and statements, there is no suggestion in the prior art of record for the entirety of the claimed invention.

Kodaira is directed to a virtual memory space that is divided into two ranges 30, 31. Kodaira teaches that a logical address 80 is divided into portions 81, 82. When the portion 81 is all zeros, a first segment table 11 is used to translate the logical address into an address corresponding to the range 31. When the portion 81 is not all zeros, a second segment table 12 is used to translate the logical address into an address corresponding to the range 30. See, Kodaira, Figures 1 and 2 and related discussion. However, as admitted by the Examiner, Kodaira fails to teach using a hard mapped mechanism to generate a physical address.

Bourekas is directed to reducing a pin count of a microprocessor that includes support for byte enable and a burst address counter. Bourekas describes an on-chip control co-processor 12 that performed virtual-to-physical address mapping using kernel segments that are hard mapped to physical addresses. The virtual-to-physical address mapping also includes kernel and user segments that are mapped page-by-page by a translation lookaside buffer into anywhere in the four gigabyte address space. Bourekas teaches that deterministic response in real-time applications is insured by locking eight pages in the translation lookaside buffer. See Bourekas, col. 3, ll. 3-16. However, contrary to the Examiner's allegations, Bourekas does not appear to teach that there is any particular advantage to performing virtual-to-physical address mapping using kernel segments that are hard mapped to physical addresses.

Moreover, the cited references provide no suggestion or motivation to combine the teachings of the cited references in the manner proposed by the Examiner. To the contrary, Kodaira and Bourekas are concerned with completely different problems: Kodaira is concerned

with efficient use of memory space and Bourekas is concerned with reducing pin count. Thus, neither Kodaira nor Bourekas teach or suggest any problem with the prior art that may be solved by, or any advantages that may accrue from, combining the teachings of the references in the manner proposed by the Examiner. In particular, the cited references fail to provide any suggestion or motivation for combining kernel segments that are hard mapped to physical addresses (as taught by Bourekas) with the memory addressing scheme taught by Kodaira. The only suggestion for the entirety of the claimed invention is found in Applicants' specification and Applicants therefore submit that the Examiner has improperly used hindsight in alleging that the present invention is obvious over the cited references.

In rejecting claims 5-9 and 15-16, the Examiner relies upon Christenson to teach executing program instructions that are stored in a main memory. Christenson is directed to providing simultaneous local and global addressing capabilities in a computer system. Christenson notes that virtual addressing schemes map virtual address spaces onto physical (real) address spaces. See Christenson, col. 1, ll. 49-59. Christenson also teaches translating a virtual address to a physical address using a page table if the virtual address is not out of range, i.e. if the virtual address does not span beyond a segment (subdivision) boundary defined within the global addresses. However, if the virtual address is out of range, an interrupt is generated to indicate an addressing error. A page fault routine may also be called to try to load a page into memory. See Christenson, col. 10, ll. 51-63. Thus, Christenson appears to teach away from the claimed invention by teaching that an interrupt is generated in response to determining that the virtual address is out of range. In particular, Christenson appears to teach away from using a paging mechanism to generate a first physical address from the virtual address in response to the virtual address being outside the first preselected range. It is by now well established that

teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

Applicants note that the Examiner has provided no detailed explanation for the rejection of claim 10 set forth in the Office Action Summary. Applicants respectfully submit that, for at least the aforementioned reasons, claim 10 is allowable over the prior art.

For at least the aforementioned reasons, Applicants respectfully submit that claims 1, 11, 12, and all claims depending therefrom are not obvious over the cited references, either alone or in combination, and request that the Examiner's rejection of claims 1, 4-12, and 15-16 under 35 U.S.C. § 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: 11/9/04

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